10/605,544

1. (Currently Amended) A split-gate fin-type field effect transistor (FinFET) comprising:

a plurality of parallel fin structures;

back gate conductors ~~between channel regions of alternating pairs of~~ adjacent said fin structures; and

front gate conductors ~~between channel regions of opposite alternating pairs of~~ adjacent said fin structures,

wherein said back gate conductors and said front gate conductors are alternatively interdigitated between channel regions of said fin structures such that each of said channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the other side of said fin structure.

2. (Currently Amended) ~~The split-gate FinFET in claim 1, further comprising:~~ A split-gate fin-type field effect transistor (FinFET) comprising:

a plurality of parallel fin structures;

back gate conductors between channel regions of alternating pairs of said fin structures;

front gate conductors between channel regions of opposite alternating pairs of said fin structures;

a back gate wiring layer connected to said back gate conductors;

a front gate wiring layer connected to said front gate conductors;

a first insulator layer positioned between said front gate conductors and said back gate wiring layer; and

a second insulator layer positioned between said back gate conductors and said front gate wiring layer.

3. (Original) The split-gate FinFET in claim 2, further comprising:

a first conductive via connected to said back gate wiring layer; and

a second conductive via connected to said front gate wiring layer.

4. (Original) The split-gate FinFET in claim 2, wherein said front gate conductors and said front gate wiring layer comprise a continuous conductive unitary structure.

5. (Original) The split-gate FinFET in claim 1, wherein ones of said front gate conductors are positioned adjacent to outer sides of channel regions of end fin structures of said split gate FinFET.

6. (Original) The split-gate FinFET in claim 1, further comprising gate insulators between said back and front gate conductors and said channel regions.

7. (Original) The split-gate FinFET in claim 1, wherein said back gate controls the threshold voltage level of said split-gate FinFET.

8. (Original) A split-gate fin-type field effect transistor (FinFET) comprising:

a plurality of parallel fin structures, wherein each of said fin structures comprises a source region in a first end of said fin, a drain region in a second end of said fin, and a channel region in a middle portion of said fin between said first end and said second end;

back gate conductors between channel regions of alternating pairs of said fin structures;

front gate conductors between channel regions of opposite alternating pairs of said fin structures, such that said back gate conductors and said front gate conductors are alternatively interdigitated between channel regions of said fin structures and such that each of said channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the other side of said fin structure;

a well region positioned below said fin structures, wherein said well region is electrically connected to said back gate conductors; and

a front gate wiring layer positioned above said fin structures, wherein said front gate

wiring layer is electrically connected to said front gate conductors.

9. (Original) The split-gate FinFET in claim 8, further comprising:

a first insulator layer positioned between said well region and said front gate conductors; and

a second insulator layer positioned between said front gate wiring layer and said back gate conductors.

10. (Original) The split-gate FinFET in claim 8, further comprising:

a first conductive via connected to said well region; and

a second conductive via connected to said front gate wiring layer.

11. (Original) The split-gate FinFET in claim 8, wherein said front gate conductors and said front gate wiring layer comprise a continuous conductive unitary structure.

12. (Original) The split-gate FinFET in claim 8, wherein ones of said front gate conductors are positioned adjacent to outer sides of channel regions of end fin structures of said split gate FinFET.

13. (Original) The split-gate FinFET in claim 8, further comprising gate oxides between said back and front gate conductors and said channel regions.

14. (Original) The split-gate FinFET in claim 8, wherein said back gate controls the threshold voltage level of said split-gate FinFET.

15. (Original) A split-gate fin-type field effect transistor (FinFET) comprising:

a plurality of parallel fin structures, wherein each of said fin structures comprises a source region in a first end of said fin, a drain region in a second end of said fin, and a channel region in

a middle portion of said fin between said first end and said second end;

back gate conductors between channel regions of alternating pairs of said fin structures;

front gate conductors between channel regions of opposite alternating pairs of said fin structures, such that said back gate conductors and said front gate conductors are alternatively interdigitated between channel regions of said fin structures and such that each of said channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the other side of said fin structure;

a back gate wiring layer positioned below said fin structures, wherein said back gate wiring layer is electrically connected to said back gate conductors; and

a front gate wiring layer positioned above said fin structures, wherein said front gate wiring layer is electrically connected to said front gate conductors.

16. (Original) The split-gate FinFET in claim 15, further comprising:

a first insulator layer positioned between said back gate wiring layer and said front gate conductors; and

a second insulator layer positioned between said front gate wiring layer and said back gate conductors.

17. (Original) The split-gate FinFET in claim 15, further comprising:

a first conductive via connected to said back gate wiring layer; and

a second conductive via connected to said front gate wiring layer.

18. (Original) The split-gate FinFET in claim 15, wherein said front gate conductors and said front gate wiring layer comprise a continuous conductive unitary structure.

19. (Original) The split-gate FinFET in claim 15, wherein ones of said front gate conductors are positioned adjacent to outer sides of channel regions of end fin structures of said split gate FinFET.

20. (Original) The split-gate FinFET in claim 15, further comprising gate insulators between said back and front gate conductors and said channel regions.

21. (Original) The split-gate FinFET in claim 15, wherein said back gate controls the threshold voltage level of said split-gate FinFET.

22-41. (Canceled).